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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/660,484	09/12/2000	Yasuo Tanaka	OKI 262	6834

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EXAMINER
SHUKLA, RAVINDRA B

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 12/21/2001

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/660,484	Applicant(s) TANAKA, YASUO	
	Examiner Ravi B Shukla	Art Unit 2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 April 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and10-15* is/are rejected.

7)☒ Claim(s) *7-9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This Office Action is in response to an application filed on 09-12-2000 with foreign priority date of 01-19-2000 is acknowledged.

Claim Rejections - 35 USC § 112

2.The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 7-9 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In particular in claims 7-9, lines 2-3, there is no antecedent basis for "the temperature". It is unclear what temperature is being referred to. It appears to be referring "the heating temperature". Appropriate correction is required.

Claim Rejections - 35 USC § 102

3.The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

4. Claims 1, 4, 14, and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Willie et al (USPN. 6,083,819) hereinafter Willie.

With respect to claim 1 Willie teaches a method of manufacturing a semiconductor device (Figs. 1-4 # 10 col. 2 line 27), when a wafer (Figs.1-4 # 12 col. 2 line 26) having a main surface (Figs 3-4 # 14 col. 3 line 4), on which a plurality of bumps (Figs. 3-4 #18 col. 3 line 14), respectively connected to a plurality of electrode pads (Figs. 3-4 # 24 and #25 col. 3 line 13), is brought into a resin molded type package (a standard practice in the art), placing a sheet encapsulating material (# 19 col. 3 line 20) containing a thermosetting resin over said wafer (# 12 col. 3 line 19) so as to cover said main surface; &heating and curing said sheet encapsulating material by a heating apparatus to form an encapsulating resin layer (Fig.4 # 20 col. 3 line 32).

With respect to claim 4 Willie teach a method of manufacturing a semiconductor device (Figs. 1-4 # 10 col. 2 line 27) and further show that heating and curing are done by heating the wafer (Fig. 4 #12) with the heating apparatus after the provision of sheet encapsulating material (# 19) over said wafer. (See col. 3 lines 31-48)

With respect to claim 14 and 15 Willie teach a method of manufacturing a semiconductor device (Figs 1 and 2 #8 col. 8 line 26), and further show that the sheet encapsulating material (Willie Fig. 3 #19 col. 3 line 20) contains a curing agent for curing thermosetting resin (epoxy resin + amine catalyst +filler silica or alumina), in a state in which curing agent is enclosed in a capsule (Willie Figs 3- 4 # 19 col. 3 line 23) broken at curing temperature to form encapsulant (Willie Fig. 4 #20 col. 3 line 32), as sheet encapsulating material (Figs 3- 4 # 20 col. 3 line 23) contains an antifoaming agent (amine catalyst +filler silica or alumina), for removing voids contained in sheet encapsulating material. (See Willie col. 3 lines 19-48).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 2 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Willie et al (USPN. 6,083,819) hereinafter Willie and further in view of King et al (USPN. 6,232,213 B1) hereinafter King.

With respect to claim 2 Willie teach a method of manufacturing a semiconductor device (Figs. 1-4 # 10 col. 2 line 27), but fail to show the steps of polishing encapsulating resin layer to thereby expose the tops of bumps after forming the encapsulating resin layer.

King show the steps of polishing encapsulating resin layer (Fig. 7 #26 col. 4 line 47) to thereby expose the tops of bumps (Fig. 7 # 34 col. 4 line50) after forming the encapsulating resin layer. (See King col. 4 lines 46-56).

Therefore it would have been obvious to one of ordinary skill in the art of making semiconductor devices to apply the teaching of King in the method of Willie to show the steps of polishing encapsulating resin layer to thereby expose the tops of bumps after forming the encapsulating resin layer, because in doing so with the facilitates connection to an external circuit and combines the small size of chip scale type

packages durability and economics of conventional lead frame assemblies and encapsulating techniques. (See King col.1 lines 65-67 and col. 2 lines 1-2)

With respect to claim 5. Willie teach a method of manufacturing a semiconductor device (Figs 1 and 2 #8 col. 8 line 26), and further show steps of heating and curing are done by heating the wafer (# 12) with the heating apparatus after the provision of sheet encapsulating material over the wafer (See col. 3 lines 19-21), but fails to teach heating is done before the provision of sheet encapsulating material over the wafer as recited in claim 5.

However, it would have been obvious to one of ordinary skill in the art to perform heating is done before the provision of sheet encapsulating material over the wafer in Willie's method because selection of any order of performing process steps is prima facie obvious in the absence of new or unexpected results. In re Burhans, 154 F. 2d 690, 69 USPQ 330 (CCPA 1946)

7. Claims 3, 6, 10, 11, 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Willie et al (USPN. 6,083,819) hereinafter Willie and further in view of Applicants Admitted Prior Art.

Referring to claim 3 Willie teach a method of manufacturing a semiconductor device (Figs. 1-4 # 10 col. 2 line 27), but fails to show forming external terminals each having conductivity so as to be connected to bumps respectively; and cutting wafer in which the formation of external terminals has been finished, into each individual chips.

Applicants Admitted Prior Art show forming external terminals [Fig. 8 (E) # 72 page 2 line 18] each having conductivity so as to be connected to bumps [Fig. 8 (E) #70 page

2 line 19] respectively; and cutting wafer in which the formation of external terminals has been finished, into each individual chips. [Fig. 8 (F) page 2 lines 19-21]

Therefore it would have been obvious to one of ordinary skill in the art of making semiconductor devices to apply the teaching of Applicants Admitted Prior Art in the method of Willie to show forming external terminals each having conductivity so as to be connected to bumps respectively; and cutting wafer in which the formation of external terminals has been finished, into each individual chips, because in doing so facilitates connection to an external circuit and facilitates formation of small size chip scale type packages.

With respect to claim 6 Willie show a method of manufacturing a semiconductor device (Figs. 1-4 # 10 col. 2 line 27), (Figs 1 and 2 #8 col. 8 line 26), and further show that heating and curing are done at greater than or equal to a curing temperature (Willie Fig. 4 100-175° C col. 3 lines 44-45) as these are the critical criteria at which the sheet encapsulating material shall be cured. (See Willie col. 3 lines 31-48), and it is obvious as per Applicants Admitted Prior Art (page 2 lines 7-10).

With respect to claim 10 Willie teach a method of manufacturing a semiconductor device (Figs. 1-4 # 10 col. 2 line 27), and further show covering of the sheet encapsulating material (# 19 col. 3 line 20) [containing a thermosetting resin] over said wafer (# 12 col. 3 line 19) [to thereby form an encapsulating resin layer Fig. 4 #20 col. 3 line 32] further show the covering of said sheet encapsulating material (# 19) is carried out by successively placing said sheet encapsulating material (# 19) over said

wafer(#12) from the end of said sheet encapsulating material, so it is inherent as shown by Applicants Admitted Prior Art (page 2 lines 1-11) that in such a process air is expelled out.

With respect to claim11 Willie teach a method of manufacturing a semiconductor device (Figs. 1-4 # 10 col. 2 line 27), but fails to show wherein the bumps are formed in such a manner that the positions thereof as viewed from the main surface side of the wafer and those of the electrode pads are inherently rendered different from one another on a plane basis.

Applicants Admitted Prior Art teaches that the bumps [Fig. 8 (E)# 72 page 2 line 17] are formed in such a manner that the positions thereof as viewed from the main surface side of the wafer [Fig. 8 (E) # 66 page 2 line 16] and those of the electrode pads [Fig. 8 (E) # 70 page 2 line 19] are inherently rendered different from one another on a plane basis.

Therefore it would have been obvious to one of ordinary skill in the art of making semiconductor devices to apply the teaching of Applicants Admitted Prior Art in the method of Willie to show the bumps are formed in such a manner that the positions thereof as viewed from the main surface side of the wafer and those of the electrode pads are inherently rendered different from one another on a plane basis, because in doing so facilitates connection to an external circuit and facilitates formation of small size chip scale type packages.

With respect to claim 12 and 13 Willie teach a method of manufacturing a semiconductor device (Figs. 1-4 # 10 col. 2 line 27), but fails to show that the external terminals are formed after the formation of a wiring metal over the sheet encapsulating material in such a manner that the positions of bumps as viewed from the main surface side of wafer and those of external terminals (bumps) are inherently different from one another on a plane basis and are formed in place of bumps.

Applicants Admitted Prior Art show that the external terminals [Fig. 8 (E)# 72 page 2 line 17] are formed after the formation of a wiring metal over the sheet encapsulating material [Fig. 8(A) # 68 page 2 line 6] in such a manner that the positions of bumps [Fig. 8 (E) # 70 page 2 line 19] as viewed from the main surface side of wafer [Fig. 8 (E) # 66 page 2 line 16] and those of external terminals (bumps) are inherently different from one another on a plane basis and are formed in place of bumps.

Therefore it would have been obvious to one of ordinary skill in the art of making semiconductor devices to apply the teaching of Applicants Admitted Prior Art in the method of Willie to show that the external terminals are formed after the formation of a wiring metal over the sheet encapsulating material in such a manner that the positions of bumps as viewed from the main surface side of wafer and those of external terminals (bumps) are inherently different from one another on a plane basis and are formed in place of bumps, because in doing so facilitates connection to an external circuit and facilitates formation of small size chip scale type packages.

Conclusion

8. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Ravi B. Shukla whose telephone number is (703) –306-0210. The examiner can normally be reached on M-F (8.00-5.00).

9. If attempts to reach the examiner are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached at (703) 308-4918.The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722

10. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956

rbs

Dec. 15, 2001

Wael Fahmy

SUPERVISORY PRIMARY EXAMINER
TECHNOLOGY CENTER 2800